



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,125	07/14/2003	Jeno Tihanyi	W&B-INF-1831	6875
7590	09/21/2004		EXAMINER	
LERNER AND GREENBERG, P.A. POST OFFICE BOX 2480 HOLLYWOOD, FL 33022-2480			NGUYEN, DANG T	
			ART UNIT	PAPER NUMBER
			2824	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/619,125	TIHANYI, JENO
Examiner	Art Unit	
Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 14 July 2003.

2a) This action is **FINAL**.                            2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-11,14, and 15 is/are rejected.

7) Claim(s) 12,13 is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 14 July 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 6/18/04.

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: Search history.

## **DETAILED ACTION**

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on July 14, 2003.
2. Claims 1 – 15 are pending in this case. Claims 1 and 6 are independent claims.

### ***Information Disclosure Statement***

3. The information disclosure statement (IDS) submitted on July 13, 2003 was filed before the mailing date of the first action on merit. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claim 1 - 5, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Okayasu, Patent No. 6,433,567 B1 – filed Apr. 21, 2000.**

**Regarding independent claim 1,** Figs. 1A and 1B of AAPA discloses a memory cell for permanently storing data, comprising: a memory material [7] capable of

assuming a first, high-resistance state and a second, low-resistance state (AAPA, page 11 lines 1-5); a heating device [5] configured to heat said memory material at different heating rates to a programming temperature (AAPA, page 11 lines 13-19), said memory material having a relatively high resistance or a relatively low resistance after cooling, depending on the heating rate (page 10 line 24 – page 11 line 19). However, AAPA fails to disclose the heating device having a switching device and a heating element in direct proximity with said memory material, and said switching device having a field-effect transistor with a drain region formed as a heating region.

Fig. 2 of Okayasu discloses heater cell is arranged evenly distributed to the whole chip of the CMOS integrated circuit. The drain and source of MOSFET1 of each heater cell are connected to the source voltage VDD and VSS.

AAPA and Okayasu are common subject matter for complementary transistors. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Okayasu's heater cell into AAPA's heating device for the purpose of generating heat evenly to the whole integrated circuit (Col. 5 lines 18-29).

**Regarding dependent claim 2,** Fig. 1 of AAPA discloses wherein said drain region comprises a highly doped contact-making region [8] for making contact with said memory material (AAPA, page 10 lines 13-15) (This is an objectivity only and the claim does not show any structure or method to support for highly doped).

**Regarding dependent claim 3**, AAPA discloses wherein said field-effect transistor is formed vertically in a substrate, and an insulation material having low thermal conductivity surrounds said field effect transistor (AAPA, page 12 line 4).

**Regarding dependent claim 4**, AAPA discloses the claimed invention except for insulation material contains a silicon compound. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a silicon compound for forming insulation material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

**Regarding dependent claim 5**, AAPA discloses the claimed invention except for wherein said insulation material is a silicon compound selected from the group consisting of silicon dioxide and silicon nitride. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a silicon compound selected from the group consisting of silicon dioxide and silicon nitride for forming insulation material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

**Claim 6 – 11, 14, and 15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Oglesbee et al., Patent No. 6,331,764 B1 – filed May 25, 2000.**

**Regarding independent claim 6**, Figs. 1A and 1B of AAPA discloses a memory cell for permanently storing data, comprising: a memory material [7] capable of

assuming a first, high-resistance state and a second, low-resistance state (AAPA, page 11 lines 1-5); a heating device [5] configured to heat said memory material at different heating rates to a programming temperature (AAPA, page 11 lines 13-19), said memory material having a relatively high resistance or a relatively low resistance after cooling, depending on the heating rate (page 10 line 24 – page 11 line 19). However, AAPA fails to disclose the heating device having a switching device and a heating element in direct proximity with said memory material, and said heating element has a diode device.

Fig. 1 of Oglesbee et al. discloses the thermal protective device [100] comprises switching devices [105, 140]. The switch [105] comprises a diode [110] in series with a thermal resistor [120] (Col 1 line 59 – Col. 2 line 6).

AAPA and Oglesbee et al. are common subject matter for complementary transistors. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Oglesbee's diode into AAPA's heating device for the purpose of protecting the diode from overtemperature due to continuous power dissipation (Col. 3 lines 39-41).

**Regarding dependent claim 7**, AAPA as applied to claims 6 above discloses every aspect of applicant's claimed invention except for wherein said diode device is a diode or a diode chain.

Fig. 1 of Oglesbee et al. discloses wherein said diode device is a diode chain [Zener diode] [110].

AAPA and Oglesbee et al. are common subject matter for complementary transistors. Therefore it would have been obvious to one having ordinary skill in the art

at the time the invention was made to incorporated Oglesbee's zener diode into AAPA's memory cell, since Oglesbee taught the benefit by pointing out that when the zener diode is subjected to continuous power dissipation, its temperature rises. As the temperature rises, the thermal resistor's impedance increases, thereby reducing the power dissipation in the zener diode (Abstract, lines 8-13).

**Regarding dependent claim 8**, AAPA as applied to claims 6 above discloses every aspect of applicant's claimed invention except for wherein said diode device is formed by a semiconductor material exhibiting functionality at a programming temperature.

Oglesbee et al. discloses zener diode implemented in a semiconductor material with functionality at a non linear positive temperature (see Col. 2 lines 33 – 37).

AAPA and Oglesbee et al. are common subject matter for heating element. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Oglesbee's temperature into AAPA's memory cell, since Oglesbee taught the benefit by pointing out that a steady sate condition will occur at the temperature point where the resistance change of the thermal resistor is balanced against reduced zener dissipation resulting from the change in resistance (Col. 3 lines 57-60).

**Regarding dependent claims 9 and 10**, AAPA as applied to claims 6 above discloses every aspect of applicant's claimed invention except for wherein said switching device is a transistor and a field-effect transistor.

Fig. 1 of Oglesbee et al. discloses the switch [140] is a P-channel field effect transistor (FET) switch.

AAPA and Oglesbee et al. are common subject matter for complementary transistors. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Oglesbee's transistor into AAPA's switching device, since Oglesbee taught the benefit by pointing out that the switch [140] may be any suitable switch capable of opening or closing in response to a control signal (Col. 1 lines 63-65).

**Regarding dependent claim 11**, AAPA as applied to claims 6 above discloses every aspect of applicant's claimed invention except for the switching device has a field-effect transistor and said diode device is formed by a layer sequence on a drain region of said field-effect transistor.

Fig. 1 of Oglesbee et al. discloses the switch [140] has a field-effect transistor and the diode device (Col. 2 lines 28 – 32).

AAPA and Oglesbee et al. are common subject matter for complementary transistors. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Oglesbee's diode device into AAPA's switching device for the purpose of protecting the current flow from the diode through the source/drain terminal.

**Regarding dependent claim 14**, Fig. 1A of AAPA discloses wherein said thermal resistor is a highly doped semiconductor layer (This is an objectivity only and the claim does not show any structure or method to support for highly doped).

**Regarding dependent claim 15, AAPA as applied to claims 6 above discloses every aspect of applicant's claimed invention except for wherein said diode device comprises one or more Zener diodes.**

Fig. 1 of Oglesbee et al. discloses wherein said diode device comprises one Zener diode [110] (Col. 2 lines 5-6).

AAPA and Oglesbee et al. are common subject matter for complementary transistors. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate Oglesbee's zener diode into AAPA's memory cell, since Oglesbee taught the benefit by pointing out that when the zener diode is subjected to continuous power dissipation, its temperature rises. As the temperature rises, the thermal resistor's impedance increases, thereby reducing the power dissipation in the zener diode (Abstract, lines 8-13).

#### ***Allowable Subject Matter***

5. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

**With respect to claim 12, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "the memory cell comprises a thermal**

resistor formed between said layer sequence of said diode device and said drain region of said field-effect transistor".

***Prior art***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ovshinsky et al.	Patent No. 5,912,839	Date of patent: Jun. 23, 1998
Kosa et al.	Patent No. 5,416,736	Date of Patent: Apr. 29, 1986
Gudesen et al.	Patent No. 6,055,180	Date of Patent: Apr. 25, 2000

***Contact Information***

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 9/17/2004



MICHAEL S. LEBENTRITT  
PRIMARY EXAMINER